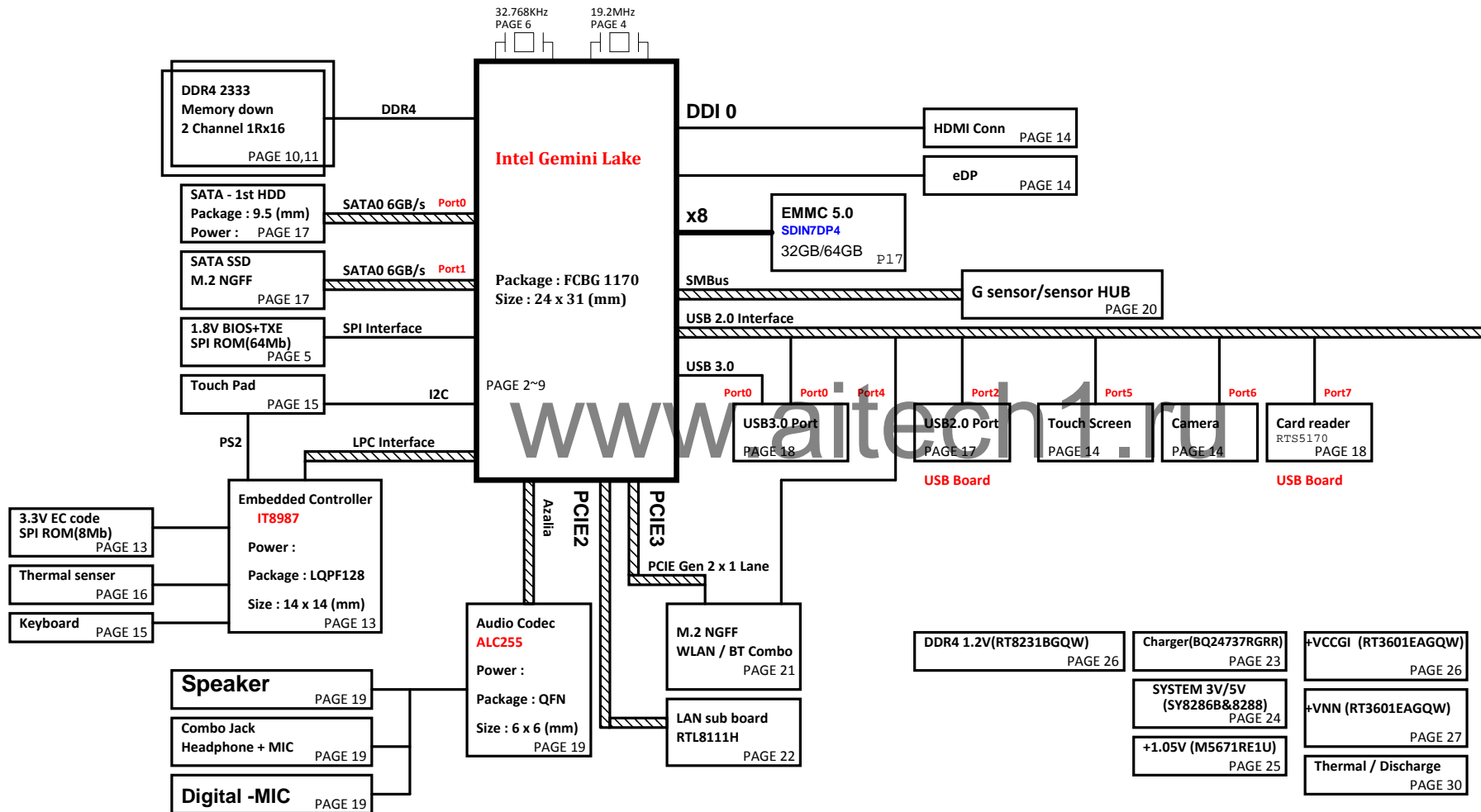
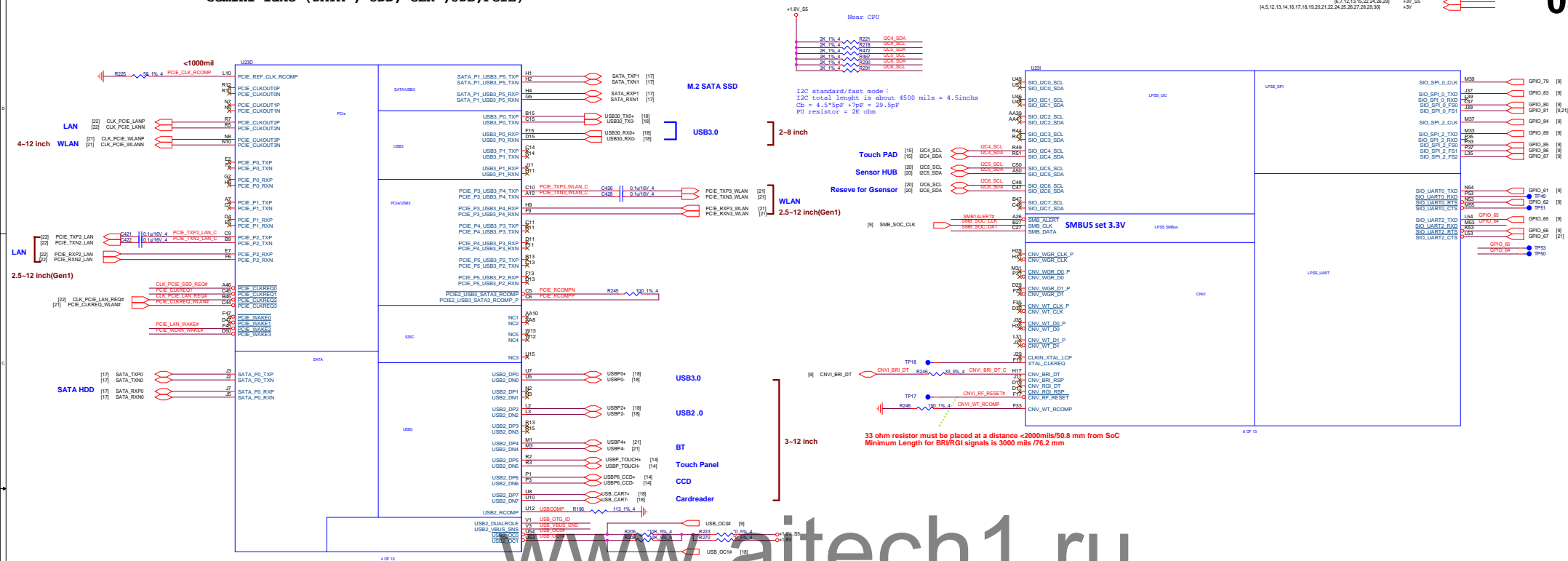


## ZHVA Virgo\_GL UMA(11.6")

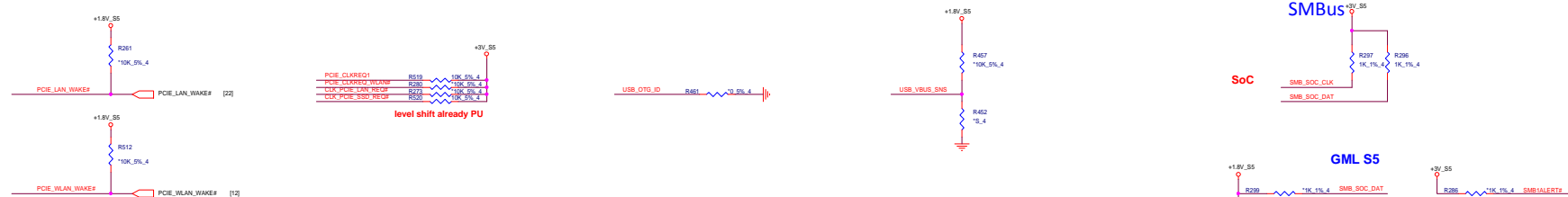
## Intel Gemini Lake Platform Block Diagram



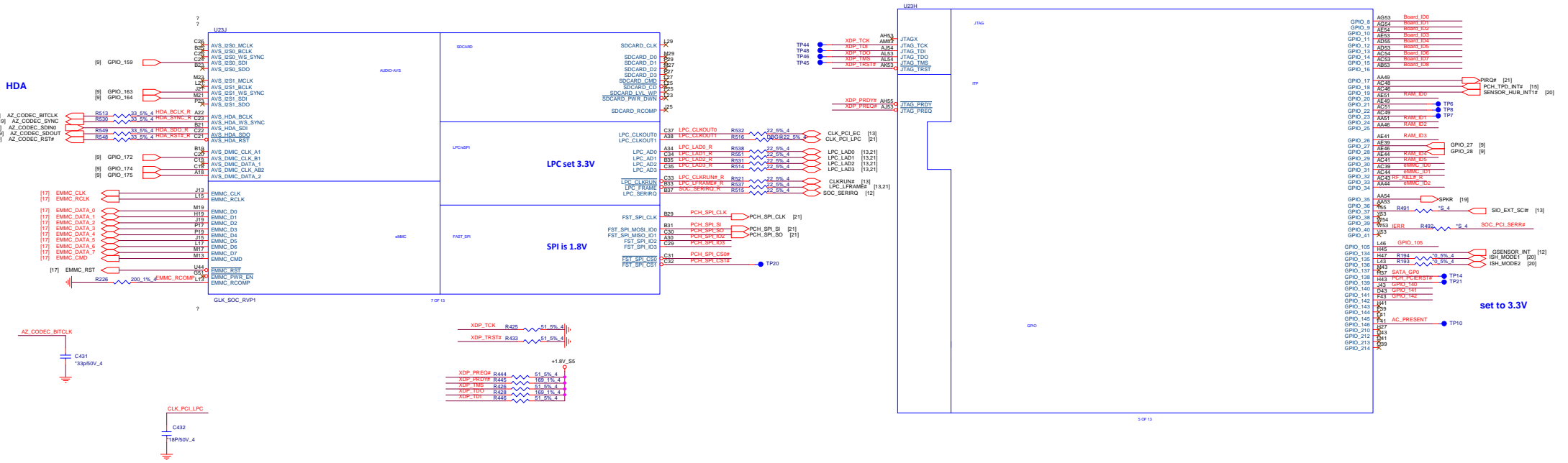




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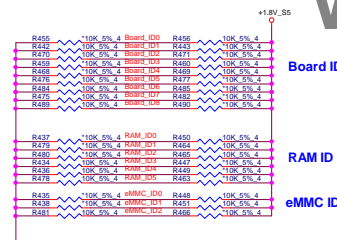
# BOARD ID SETTING

HW strap ID	Strap pin Description
Board_ID0	0 = Non Touch Screen 1 = Touch Screen
Board_ID1	0 = with eMMC 1 = Without eMMC <HDD only>
Board_ID2	0 = M.2 SATA SSD 1 = M.2 PCIe SSD
Board_ID3	0 = none G sensor 1 = G sensor
Board_ID4	0 = none TPM 1 = TPM
Board_ID5	0 = With SATA Port 0 Connector 1 = Without SATA Port 0 Connector
Board_ID6	0 = With SATA Port 1 Connector 1 = Without SATA Port 1 Connector
Board_ID7	0 = Convertible model (360°) 1 = Clamshell model
Board_ID8	Reserve
RAM_ID0	0 = Single chanel (A) 1 = Dual chanel (A&B)
RAM_ID1	0 = Channel A On board RAM 2GB 1 = Channel A On board RAM 4GB
RAM_ID2	0 = Channel B On board RAM 2GB 1 = Channel B On board RAM 4GB

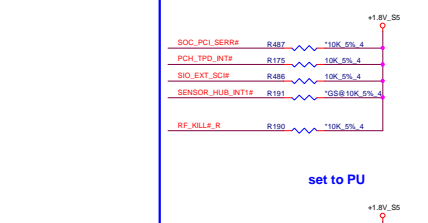
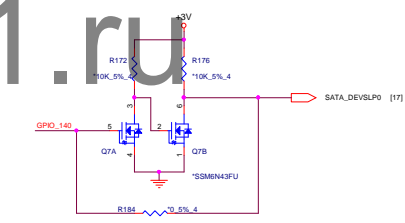
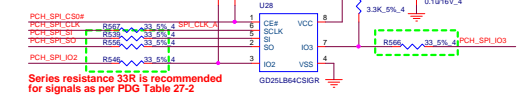
RAM_ID0	RAM_ID1	RAM_ID2	Vendor
0	0	0	Winix
0	0	1	Winix
0	1	0	Winix
0	1	1	Winix

Board_ID0	Board_ID1	Board_ID2	Vendor
0	0	0	Samsung 32/64GB
0	0	1	Winix 32/64GB
0	1	0	Winix 32/64GB
0	1	1	Winix 32/64GB

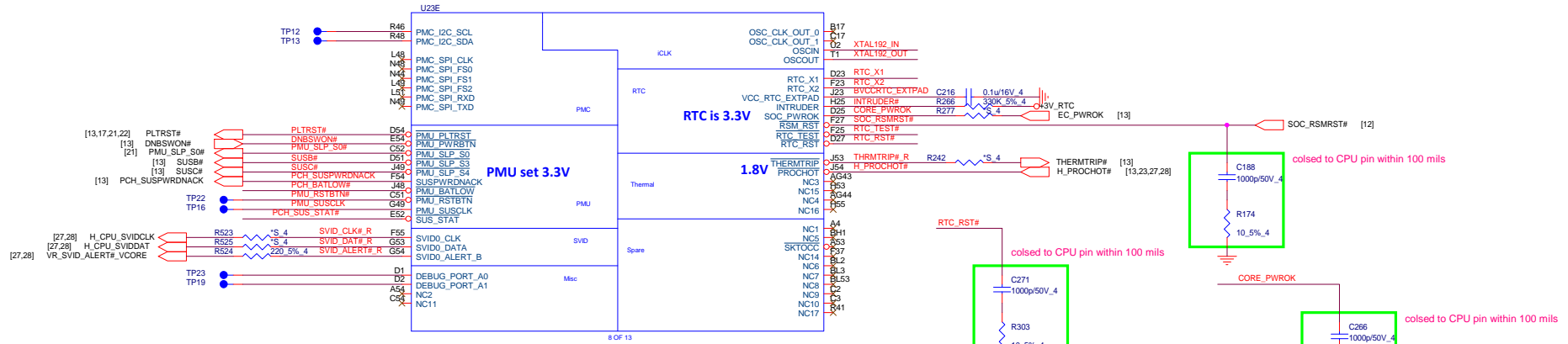
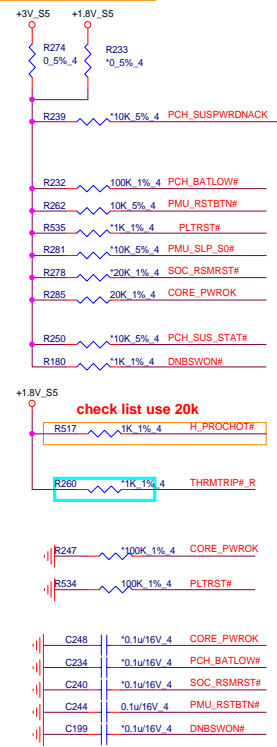
## BOARD ID SETTING



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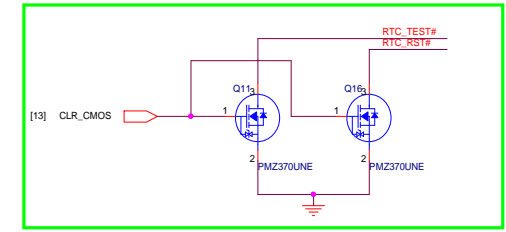


PMU set to 3.3V

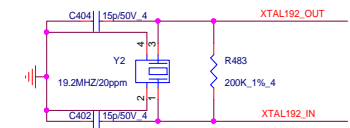
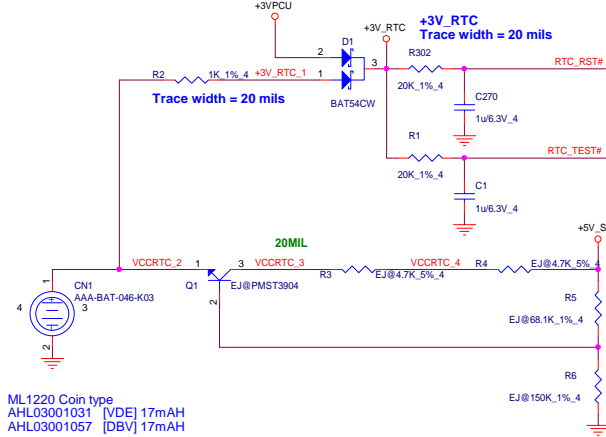


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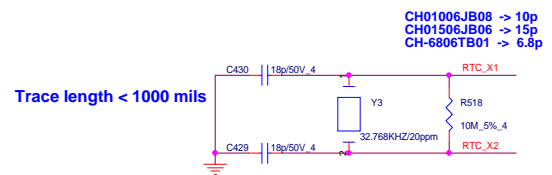
EC reset RTC



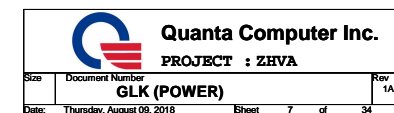
RTC Circuitry (RTC)

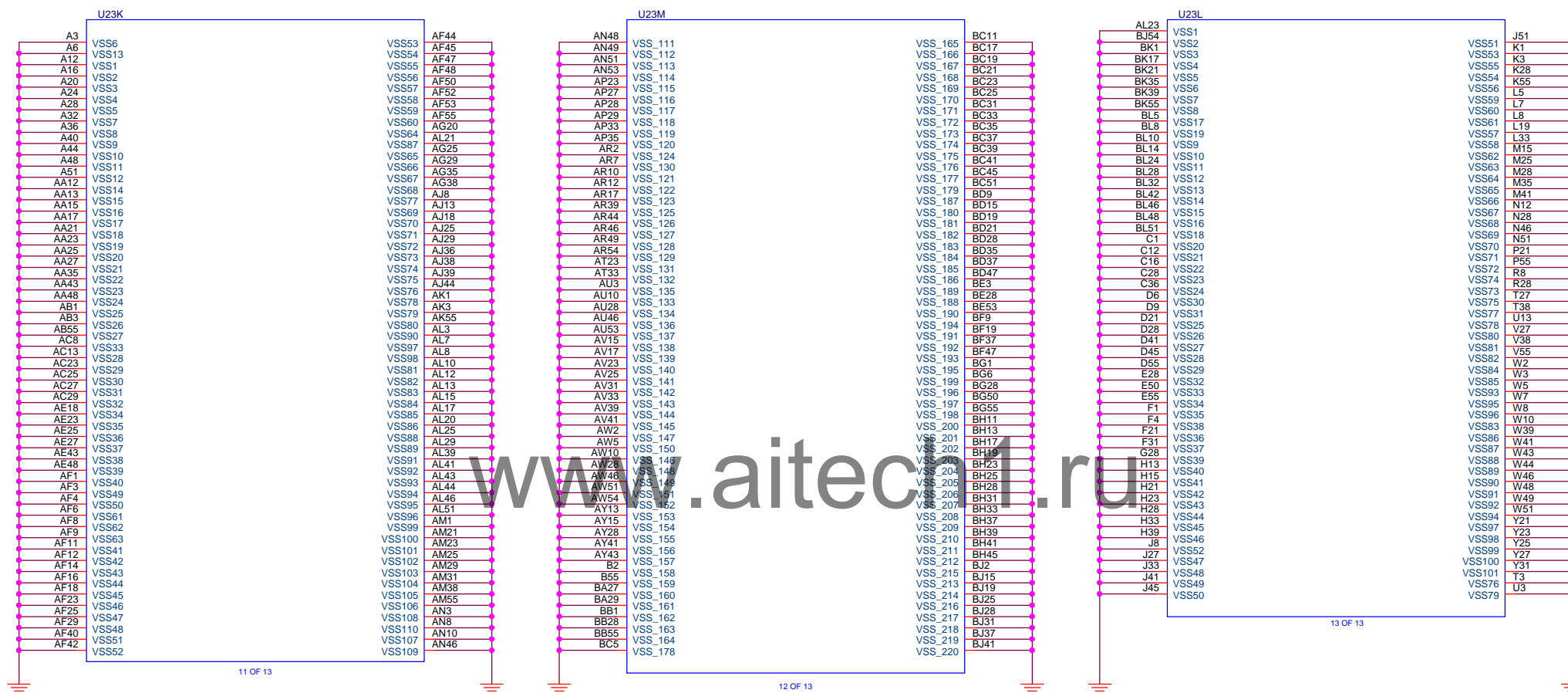


RTC Clock 32.768KHz (CPU)



Gemini (POWER)





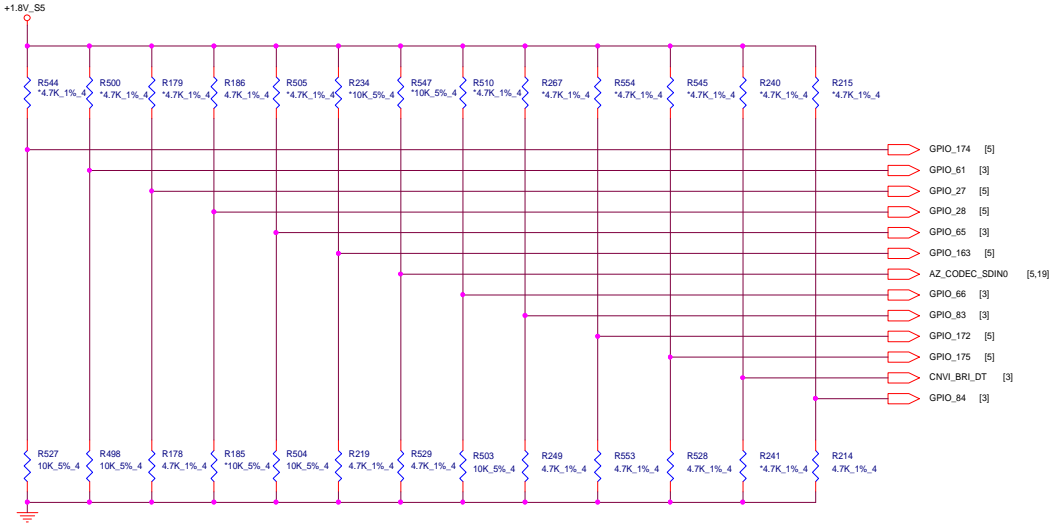
Quanta Computer Inc.

PROJECT : ZHVA

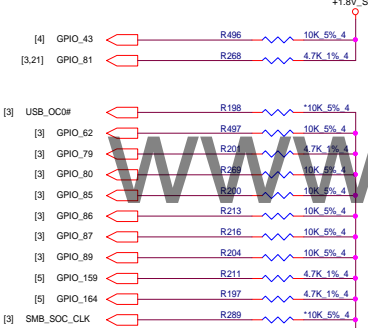
Size	Document Number	Rev
	GLK (GND)	1A
Date:	Thursday, August 09, 2018	Sheet 8 of 34



Note: If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.



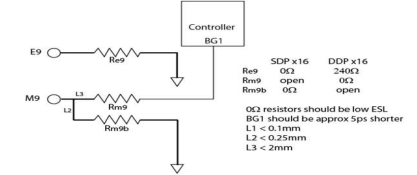
Note: The default for A0 will be eSPI due to a bug on LPC.



Hardware Strap	Strap Description	Value
GPIO_174	VDD2 1.24V vs.1.20V select 0 = 1.2V(default) 1 = 1.24V	1
GPIO_61	Enable CSE(TXE3.0) ROM Bypass 0 = Disable Bypass 1 = Enable Bypass	0
GPIO_27	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_28	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_65	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_163	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
AZ_CODEC_SDINO	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_66	LPC No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_83	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
		0
GPIO_172	SMBus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_42	Top swap override 0 = Disable 1 = Enable	0
GPIO_175	eSPI vs. LPC 0 = LPC mode (default) 1 = eSPI mode	0
CNVI_BRI_DT	eSPI Flash Sharing Mode: 0 = master attached flash sharing (MAFS; default) 1 = slave attached flash sharing (SAFS)	0
GPIO_84	Allow SPI as a boot source 0 = Enable (default) 1 = Disable	0

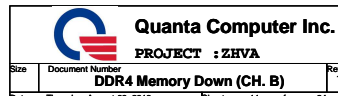
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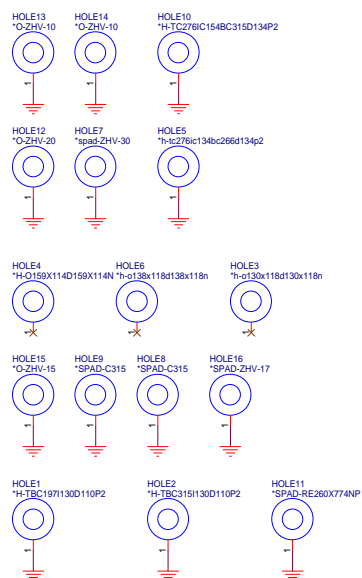
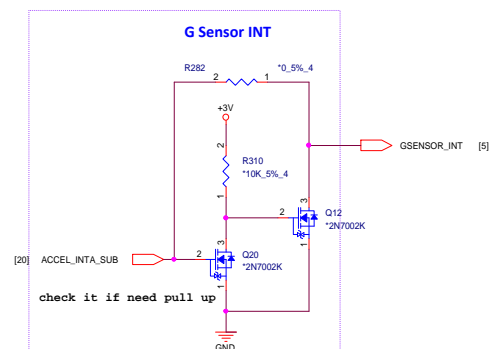
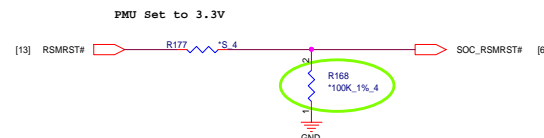
[3,4,5,6,7,12,15,21,22,23,27,29] +1.8V\_S5



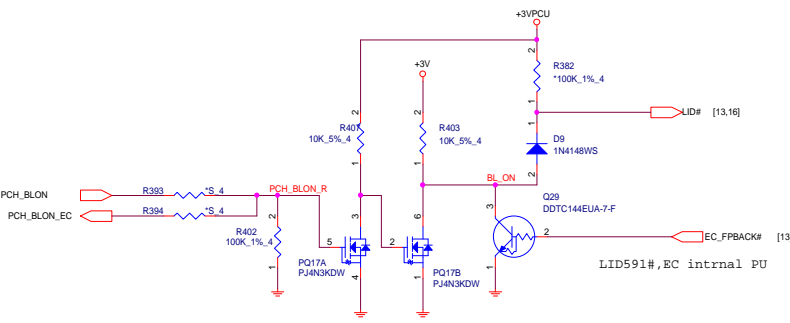
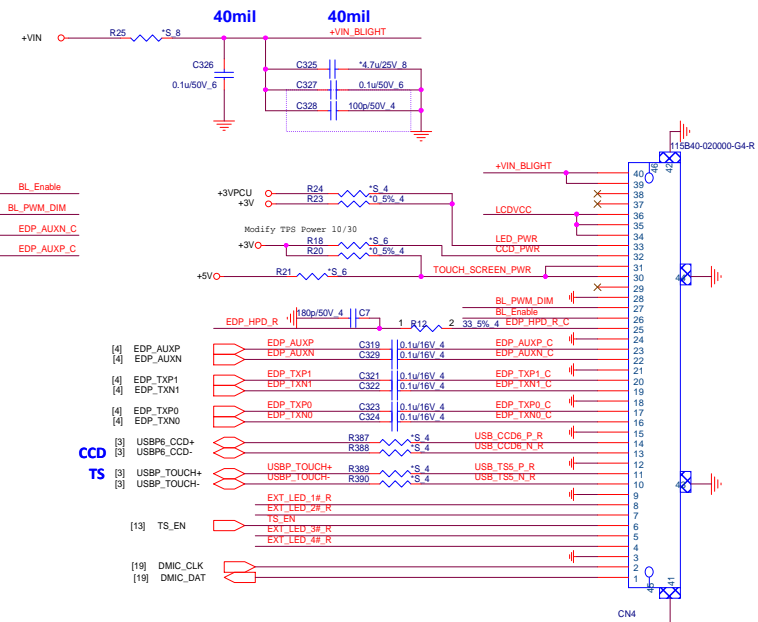
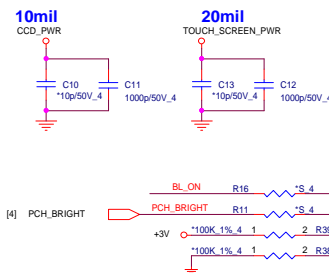
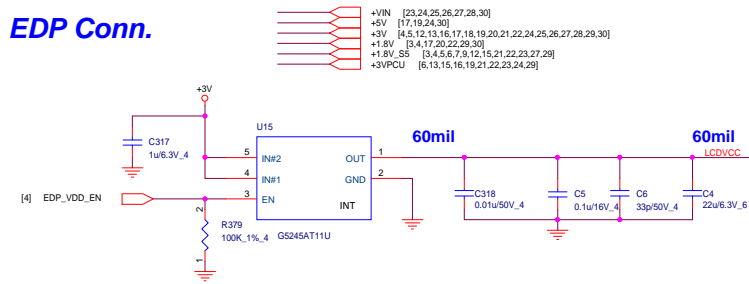


### VREF DQ1 M1 Solution

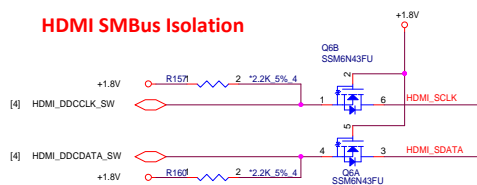






**EDP Conn.****DMI Conn.**

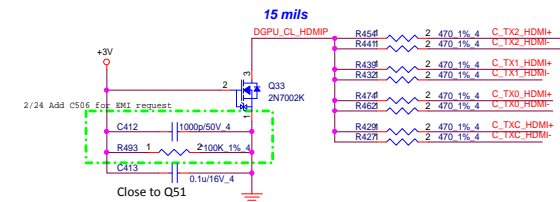
## HDMI SMBus Isolation



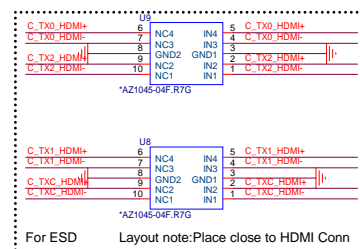
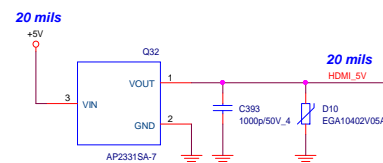
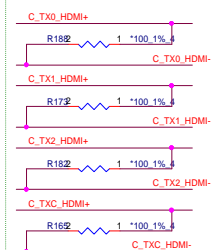
Intel Request Rds\_ON <3.5ohm

### HDMI-Level shift (HDM)

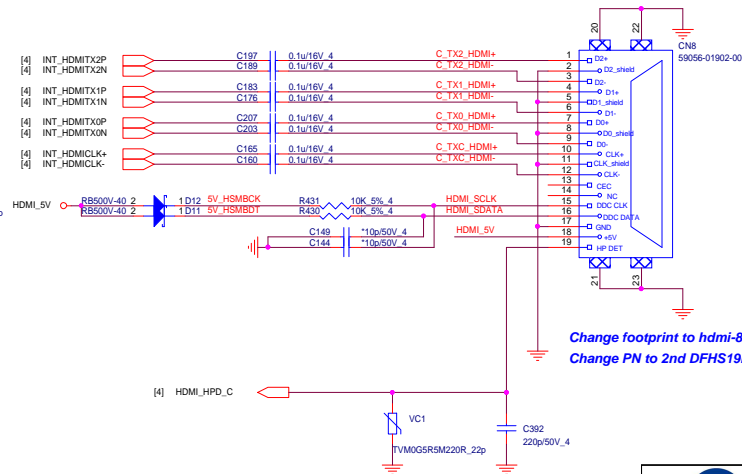
**Close to HDMI connector**



## EMI (EMC)



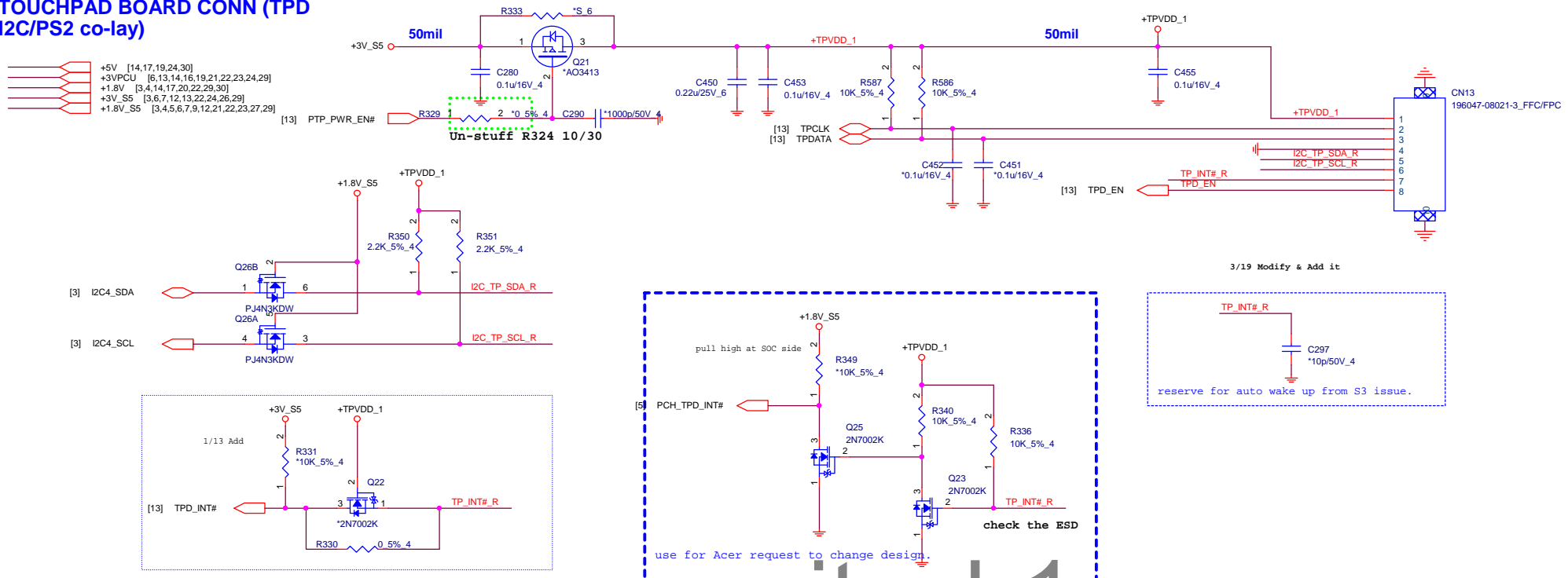
For ESD      Layout note: Place close to HDMI Conn



Change footprint to hdmi-80103-1121-19p-ldv-smt  
Change PN to 2nd DFHS19FR072 due to DFHS19FR079 SDA test fail

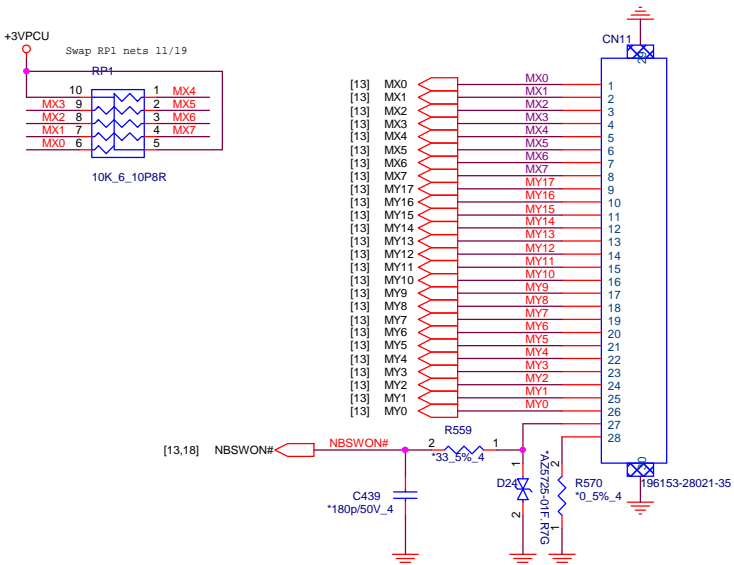
# TOUCHPAD BOARD CONN (TPD) I2C/PS2 co-lay)

15

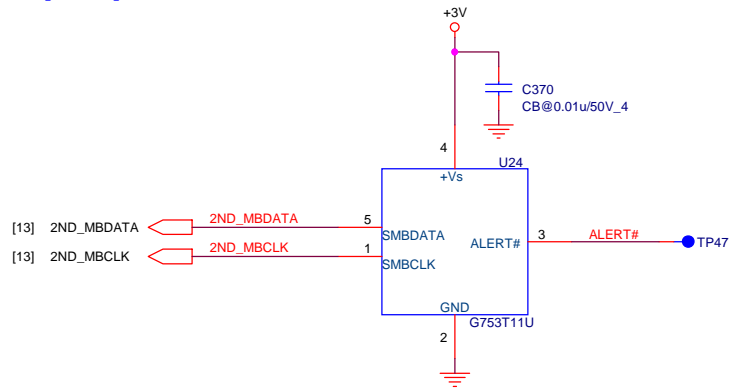


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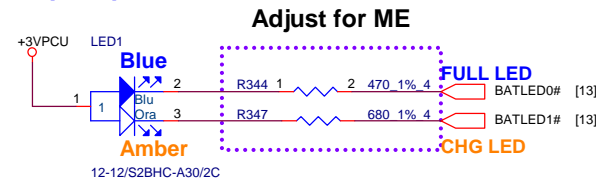
## KEYBOARD (KBC)



CPU Thermal sensor(THS) / MB Local  
TEMP (THM)



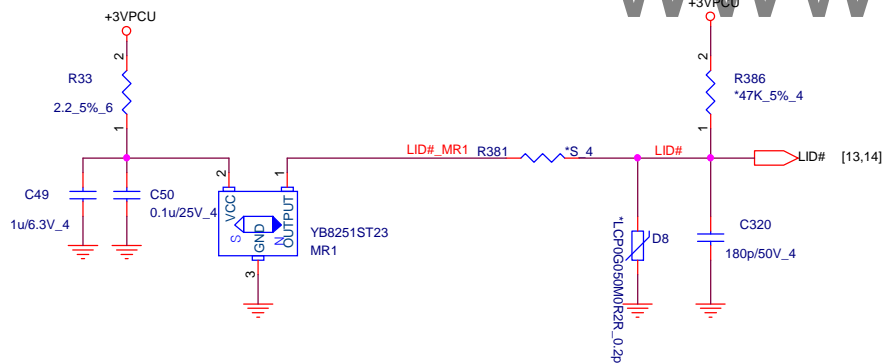
LED(UIF)



16

Del option Power SW

Lid



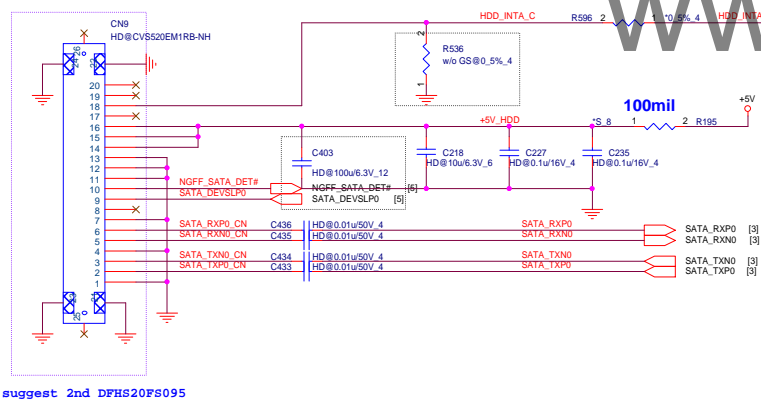
GMR(option)

Del option GMR



## 17

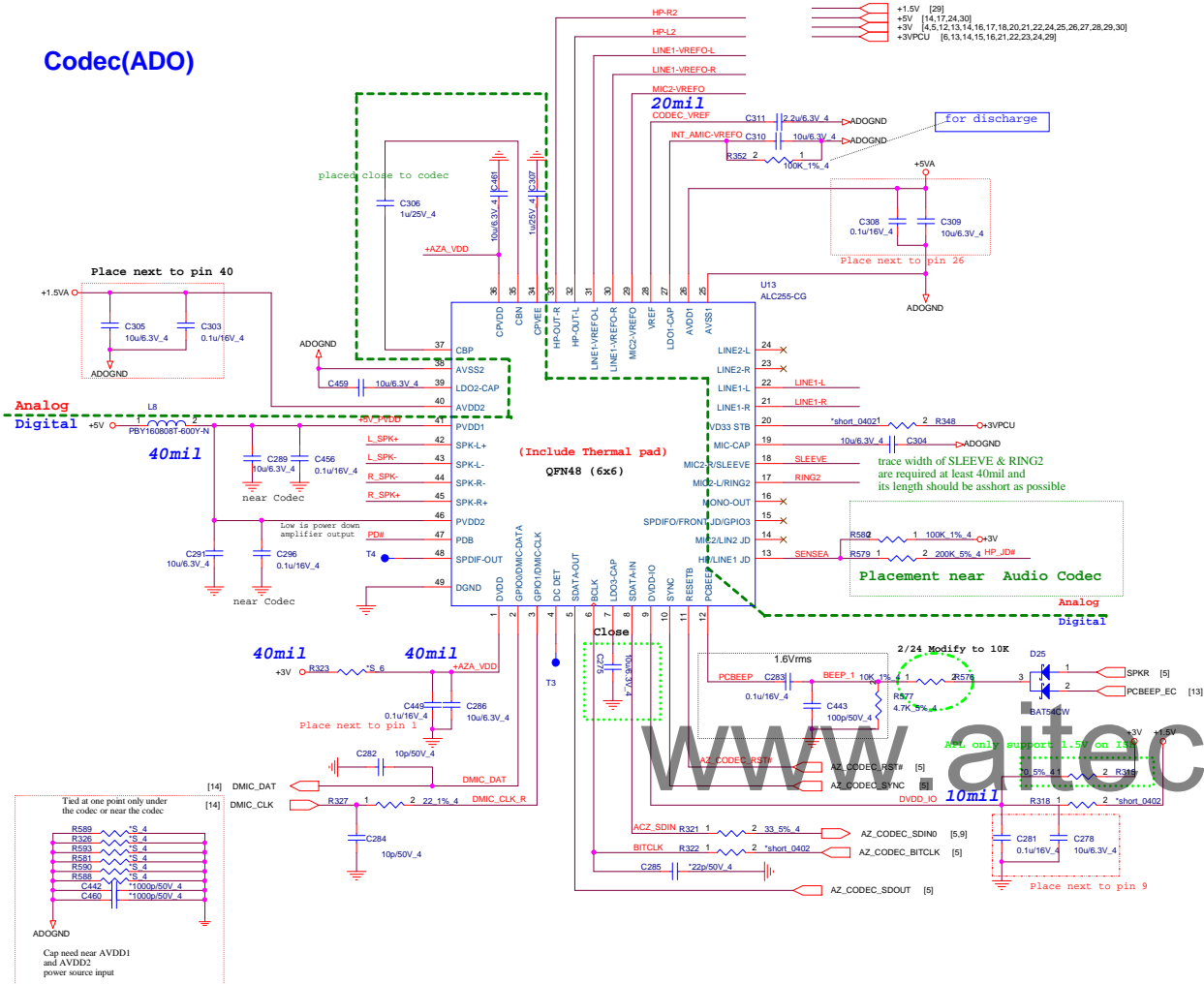
## SATA HDD



SMT suggest 2nd DFHS20FS095



## Codec(ADO)

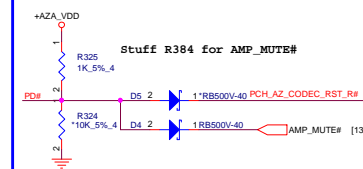


## Grounding circuit(ADO)

If IC pin20 connect to always power,  
Grounding circuit can be remove

19

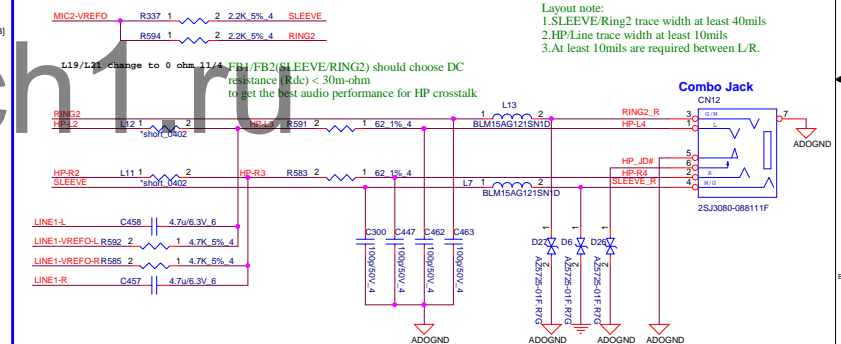
## Mute(ADO)



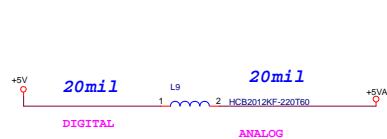
## Power (ADO)

For A-MIC LDO

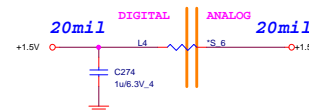
### HEADPHONE/MIC/LINE combo (ADO)



### Codec PWR 5V(ADO)

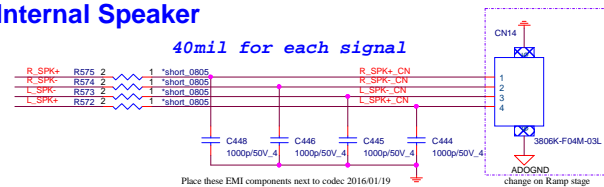


### Codec PWR 1.5V(ADO)



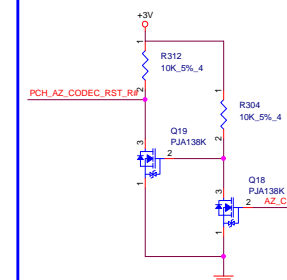
## Internal Speaker

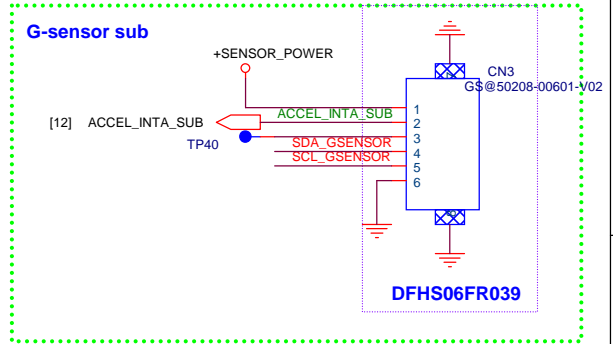
40mil for each signal



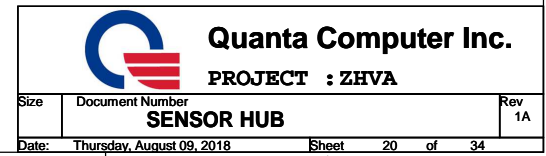
## A-Mic

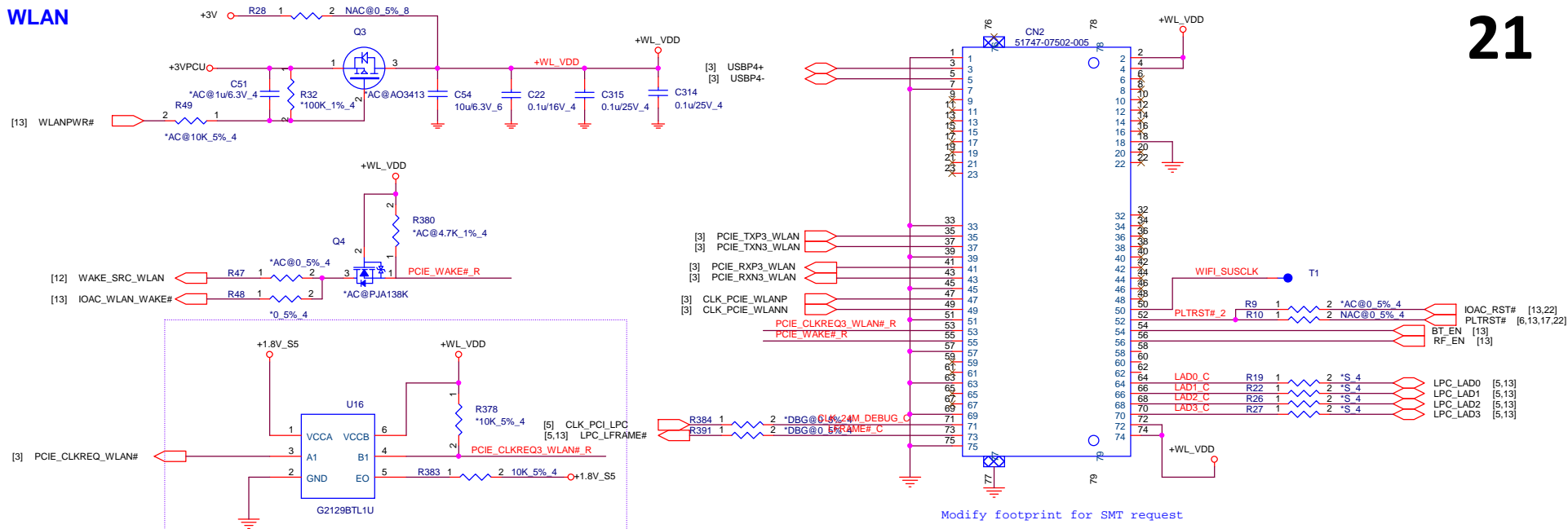
## Level shift





Pin 1 connection diagram for the ADXL345. The diagram shows the chip with pins 1 through 10. Pin 1 is connected to GND. Pin 2 is connected to VCC. Pin 3 is connected to GND. Pin 4 is connected to VCC. Pin 5 is connected to GND. Pin 6 is connected to VCC. Pin 7 is connected to GND. Pin 8 is connected to VCC. Pin 9 is connected to GND. Pin 10 is connected to VCC. The diagram also shows the internal connections of the chip, including the accelerometer core and the digital interface. A large watermark 'www.aitech1.com' is overlaid on the diagram.

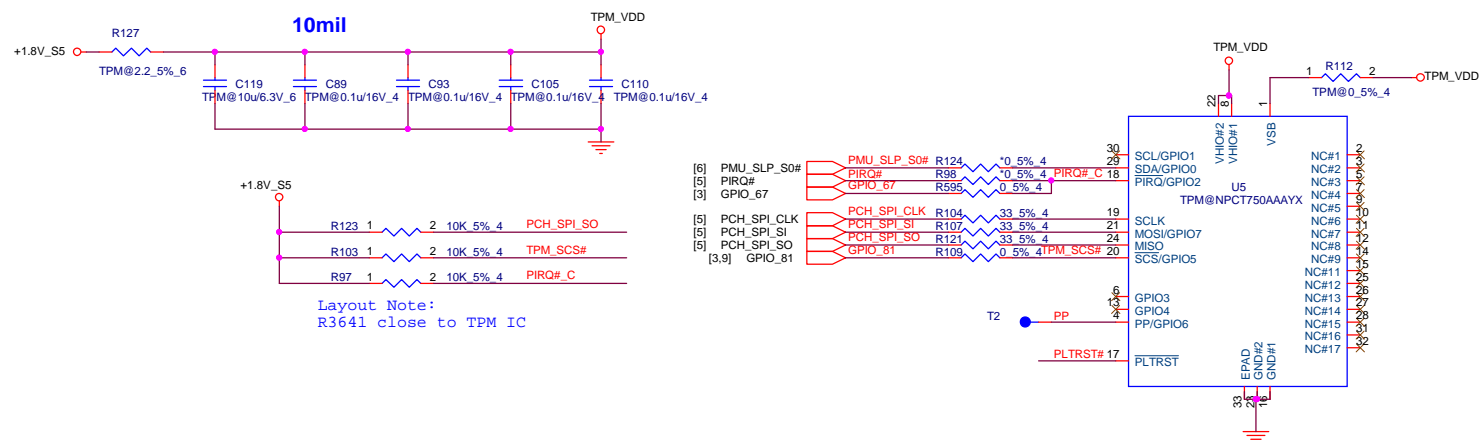




Modify footprint for SMT request

[www.aitech1.ru](http://www.aitech1.ru)

## TPM (TPM)

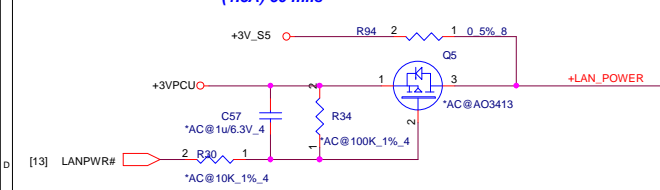


Layout Note:  
R3641 close to TPM IC

**NOTE:**

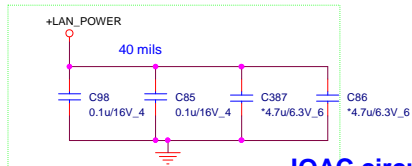
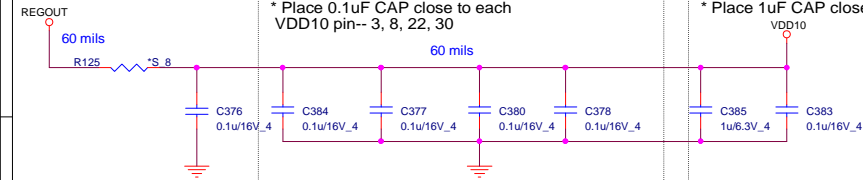
- Place 0.1 uF capacitors as close as possible to the device power pins.
- VHIO can be either +3.3V or +1.8V.
- It is recommended to connect VHIO to V\_RUN.
- VALW can be either +3.3V or +1.8V.
- VALW power rail should be powered whenever the system is powered by any power source.
- For details regarding the TPM power sequence, see the NPCT75x Datasheet and Board Design Guidelines.

## (1.5A) 60 mils



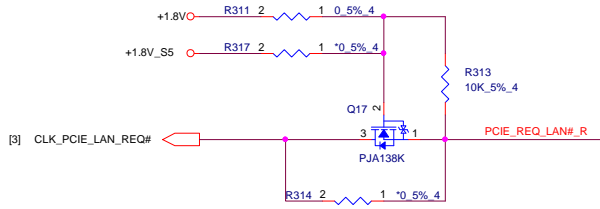
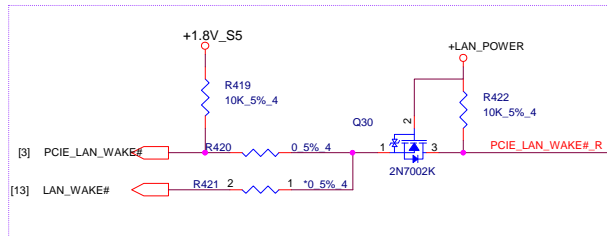
For RTL8111H  
\* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111H  
\* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

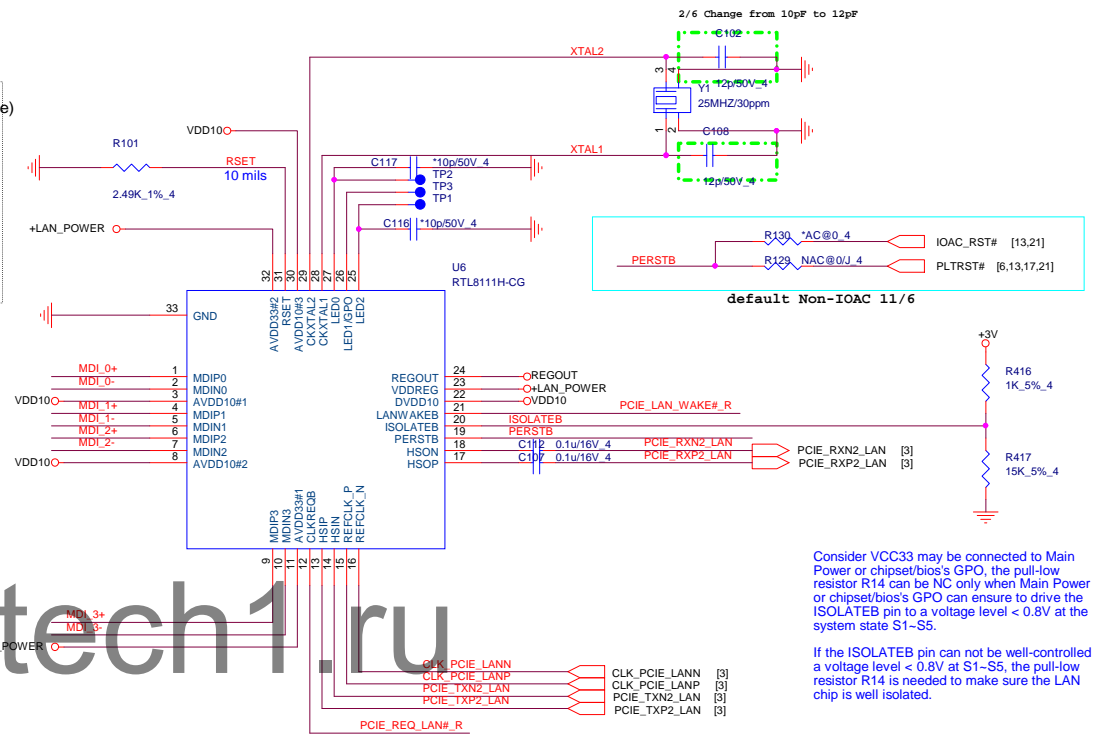


## IOAC circuit (MPC)

For RTL8111H  
\* Place 0.1uF/4.7uF CAP close to each VDD33 pin-- 11, 32



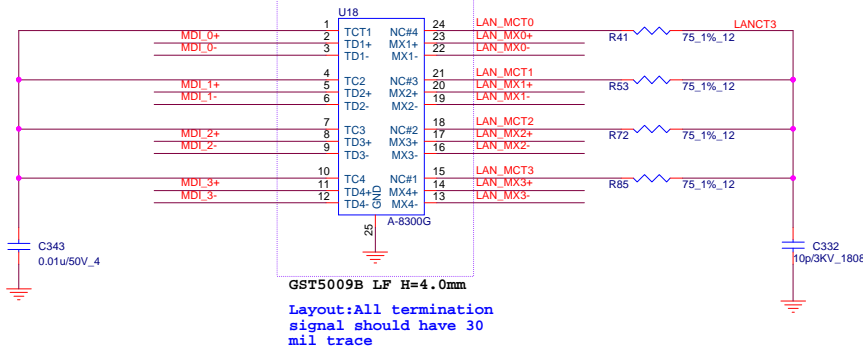
+3V [4,5,12,13,14,16,17,18,19,20,21,24,25,26,27,28,29,30]  
+3VPCU [6,13,14,15,16,19,21,23,24,29]



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATE pin to a voltage level < 0.8V at the system state S1-S5.

If the ISOLATE pin can not be well-controlled to a voltage level < 0.8V at S1-S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

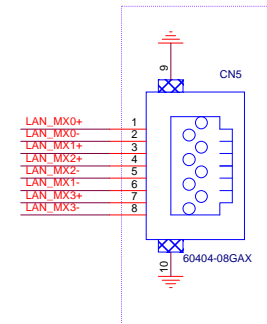
## S0 Transformer



GST5009B LF H=4.0mm

Layout: All termination signal should have 30 mil trace

## RJ45 Connector



SYMBOL AOP,PN YMI

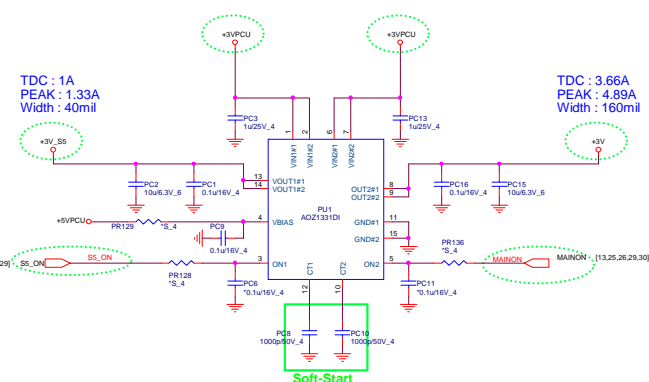


Quanta Computer Inc.

PROJECT : ZEVA

Size	Document Number	Rev
	LAN(RTL8111H-CG)	1A
Date:	Thursday, August 09, 2018	Sheet 22 of 34

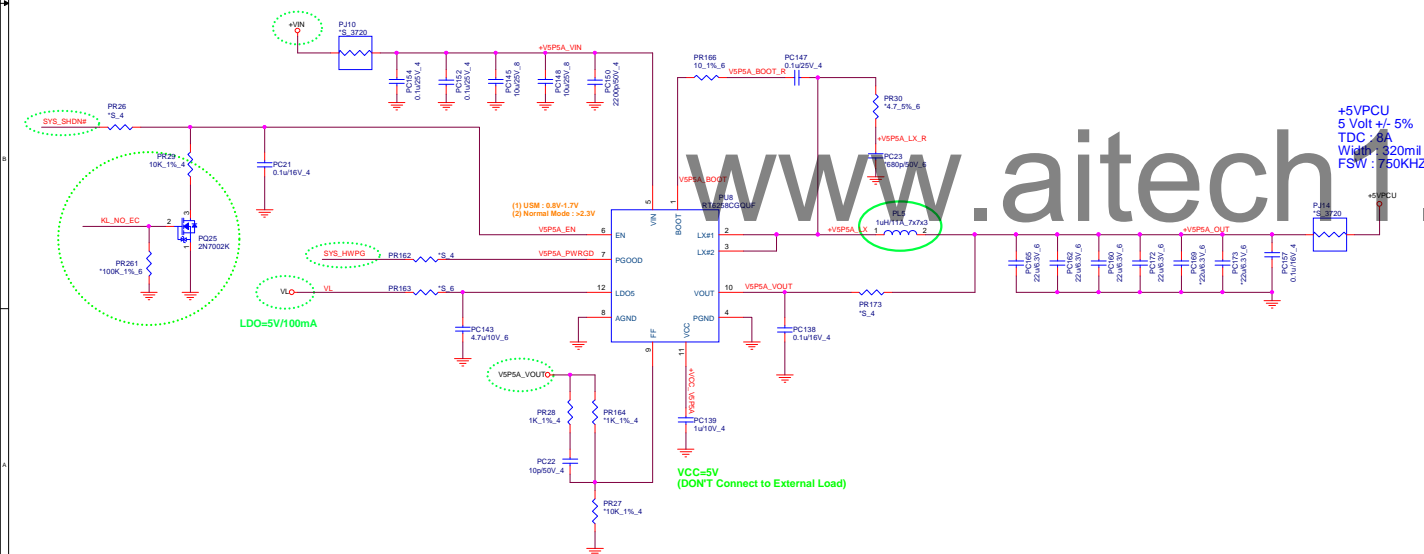




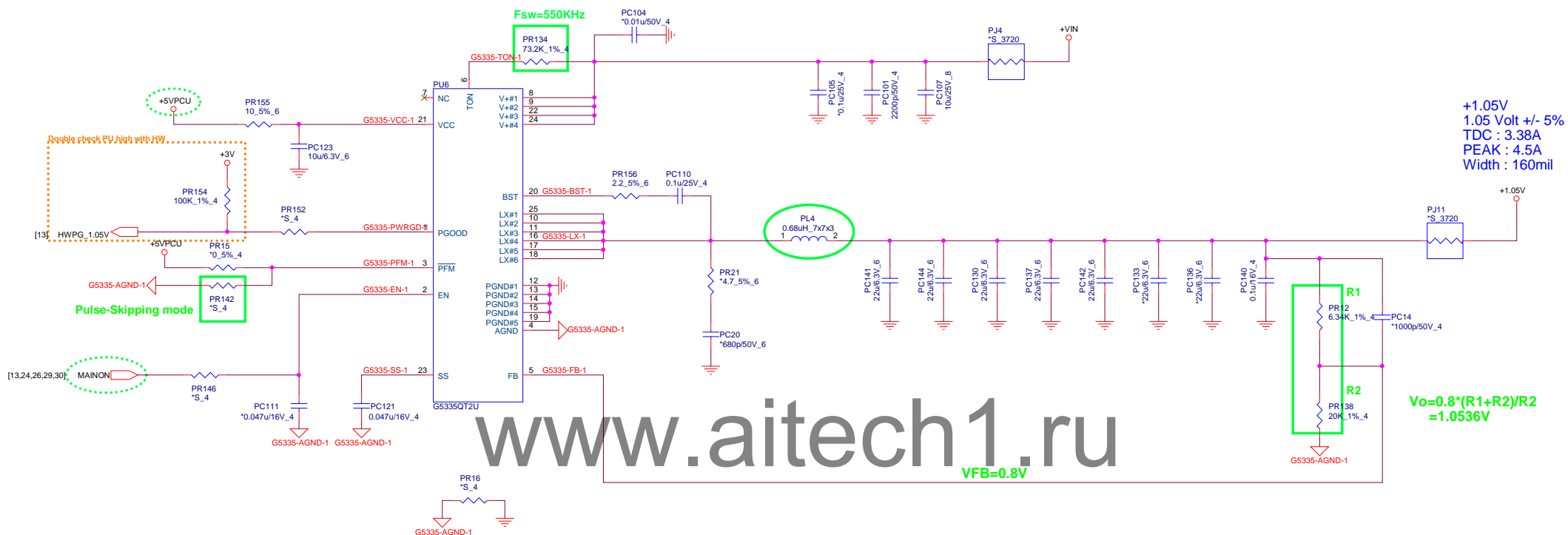
TDC: 5.25A  
PEAK: 7A  
Width: 240mil

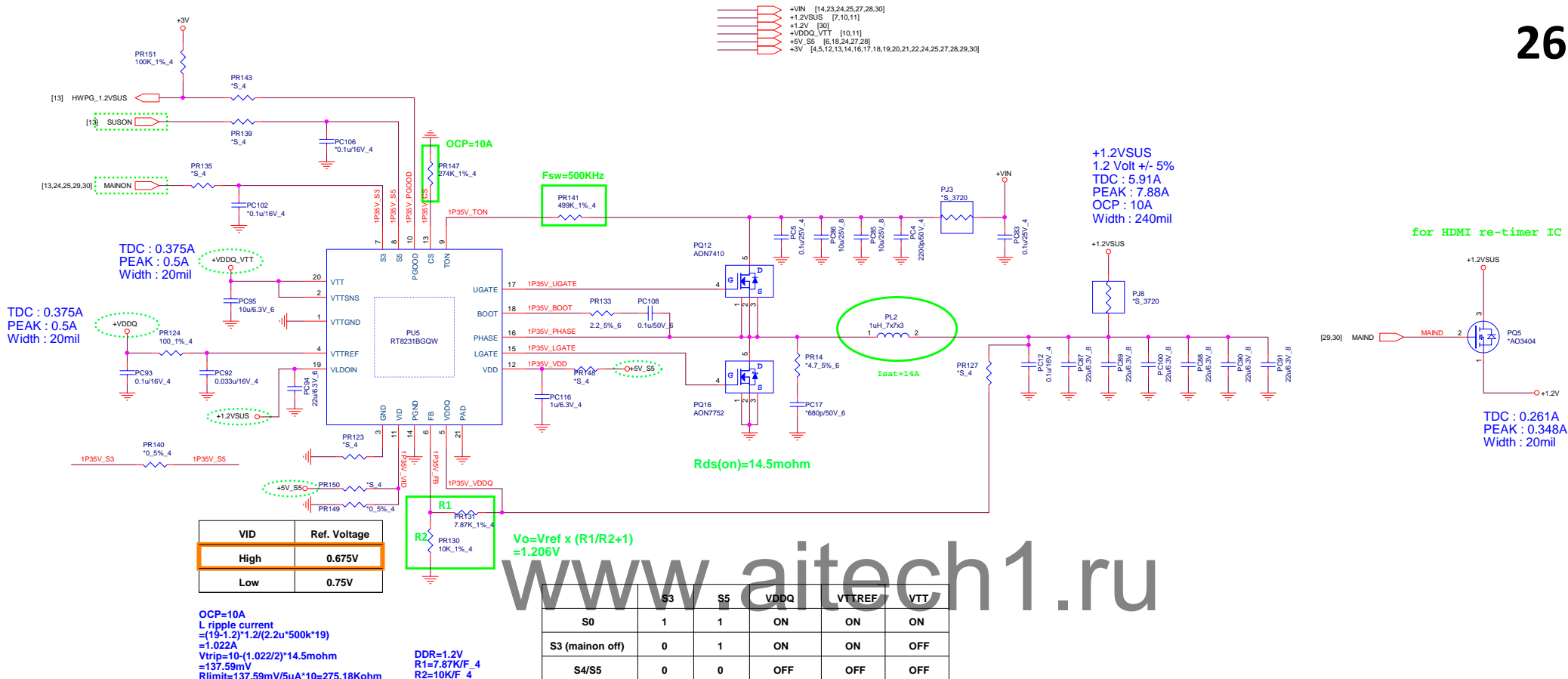
TDC: 4A  
PEAK: 5.3A  
Width: 160mil

Soft-Start

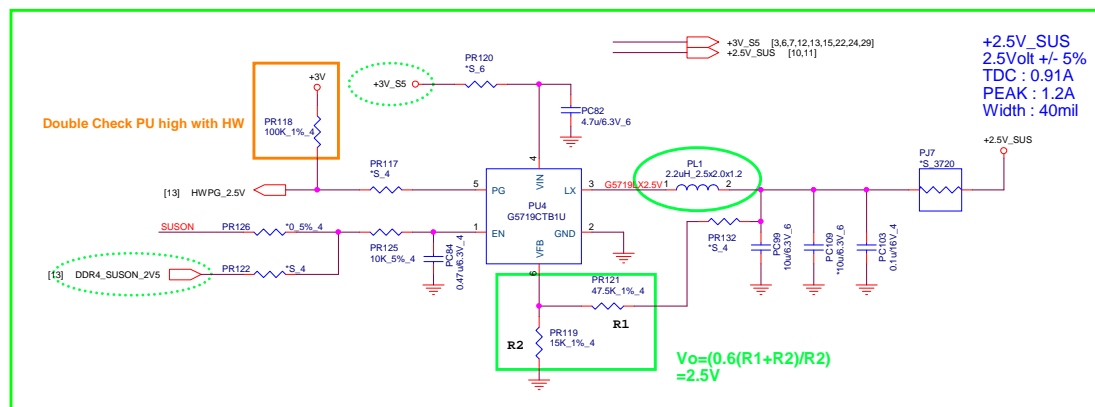




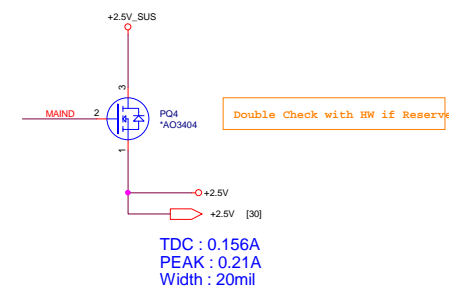




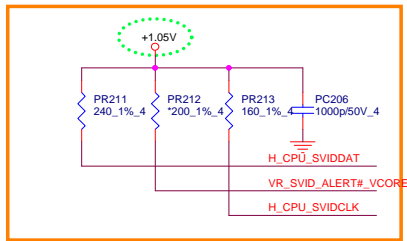
### +2.5VSUS Power Rail For DDR4



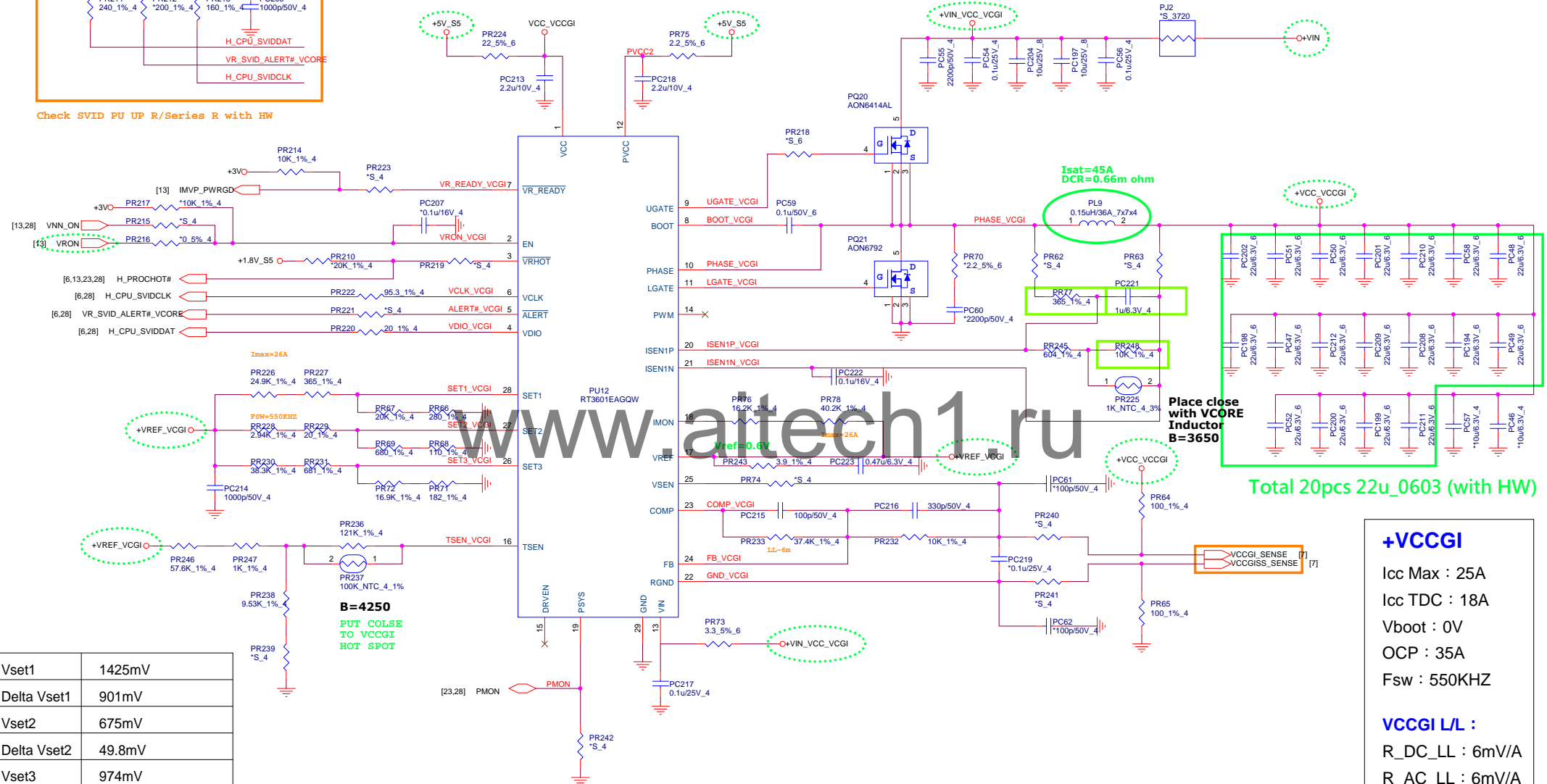
### Reserve +2.5V for DDR4 VDDSPD



SVID\_CLK : UP:160 ohm Series:95 ohm  
 SVID\_ALERT : UP:68 ohm Series:220 ohm  
 SVID\_DATA : UP:240 ohm Series:20 ohm



Check SVID PU UP R/series R with HW



Total 20pcs 22u\_0603 (with HW)

### +VCCGI

Icc Max : 25A

Icc TDC : 18A

Vboot : 0V

OCP : 35A

Fsw : 550KHZ

### VCCGI L/L :

R\_DC\_LL : 6mV/A

R\_AC\_LL : 6mV/A

Vset1	1425mV
Delta Vset1	901mV
Vset2	675mV
Delta Vset2	49.8mV
Vset3	974mV
Delta Vset3	950mV
VTsen	448mV

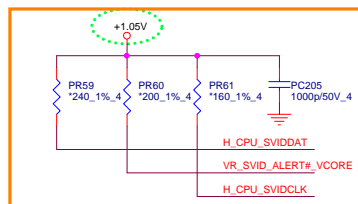


Quanta Computer Inc.

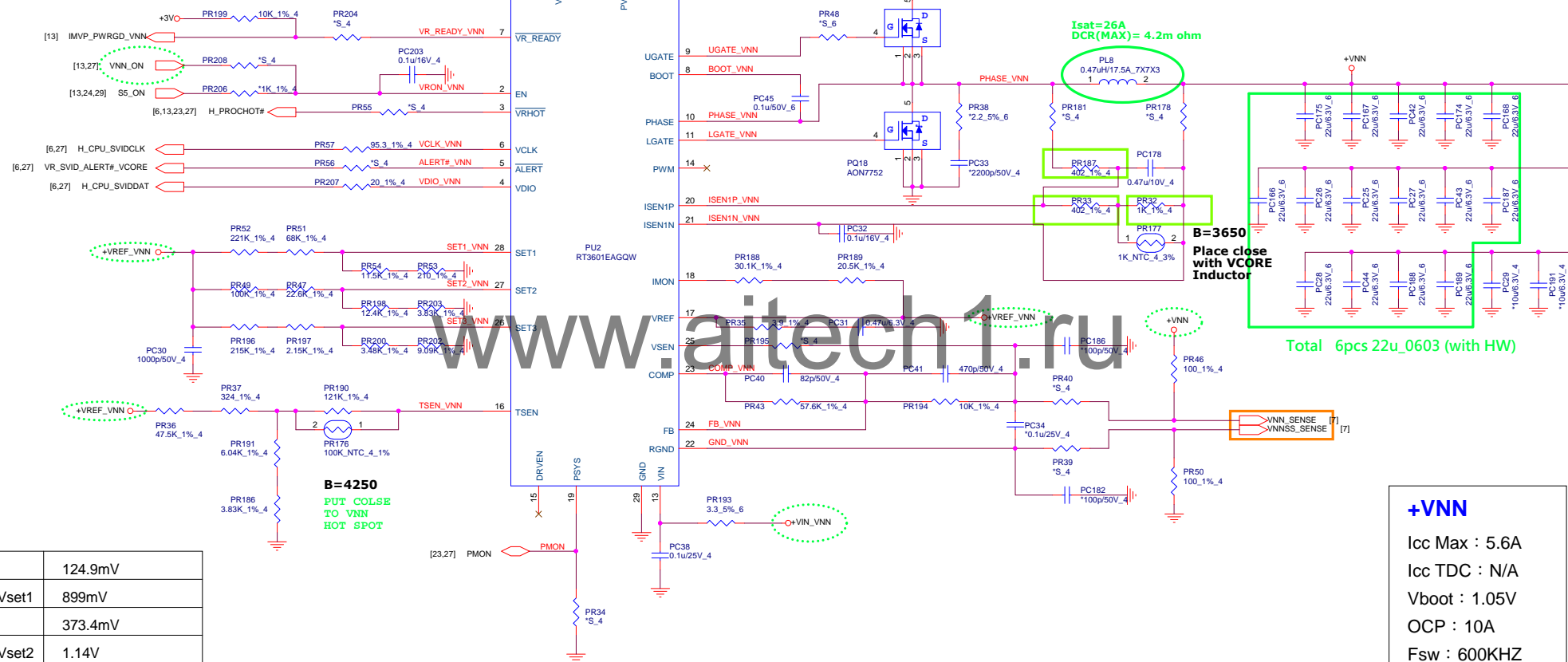
PROJECT : ZHVA

Size Document Number  
 +VCC\_VCCGI (RT3601EAGQW)  
 Date: Thursday, August 09, 2018 Sheet 27 of 34 Rev 1A

```
SVID_CLK      : UP:160 ohm   Series:95 ohm
SVID_ALERT    : UP:68 ohm    Series:220 ohm
SVID_DATA     : UP:240 ohm   Series:20 ohm
```



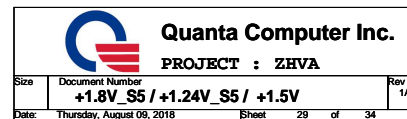
Check SVID PU UP R/Series R with HW



Vset1	124.9mV
Delta Vset1	899mV
Vset2	373.4mV
Delta Vset2	1.14V
Vset3	176mV
Delta Vset3	950mV
VTsen	548mV

**+VNN**

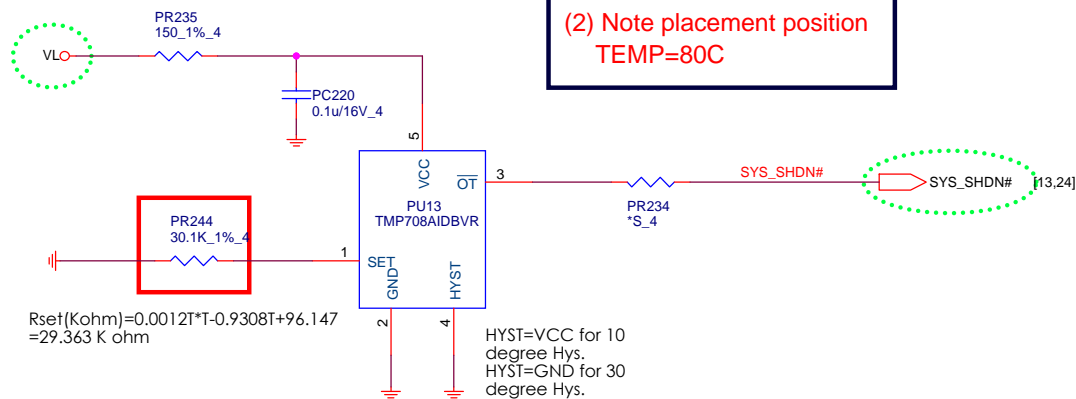
Icc Max : 5.6A  
Icc TDC : N/A  
Vboot : 1.05V  
OCP : 10A  
Fsw : 600KHZ



[24]	VL
[14,23,24,25,26,27,28]	+VIN
[4,5,12,13,14,16,17,18,19,20,21,22,24,25,26,27,28,29]	+3V
[14,17,19,24]	+5V
[3,4,14,17,20,22,29]	+1.8V
[26]	+2.5V

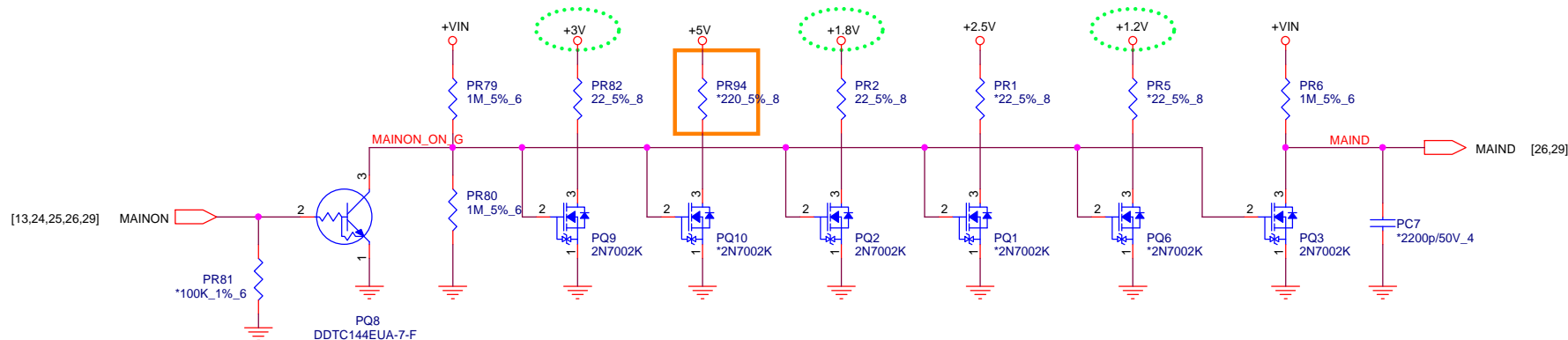
## Thermal Protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position  
TEMP=80C



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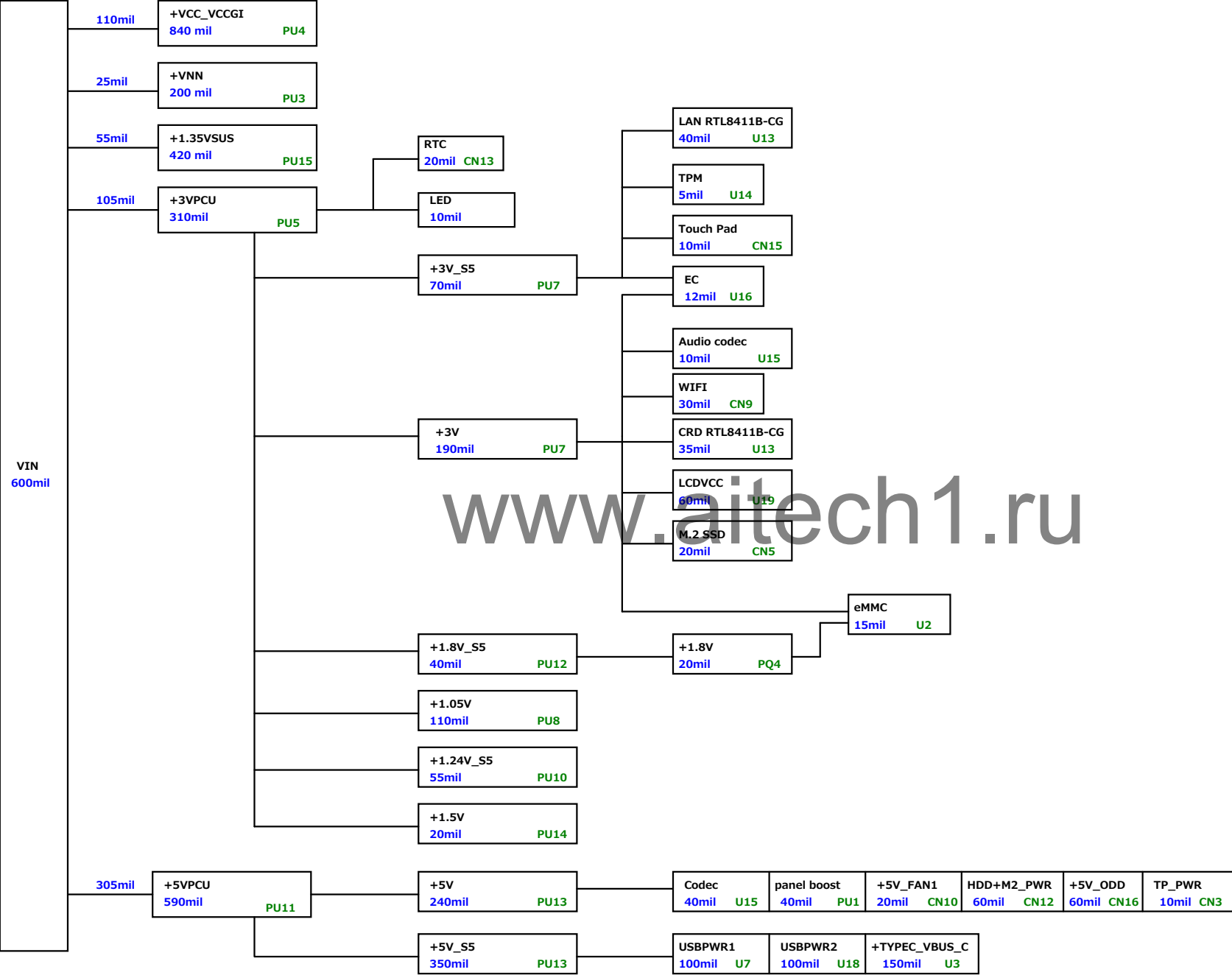
+5V PU High R= 220 ohm for Bo-Bo sound issue.

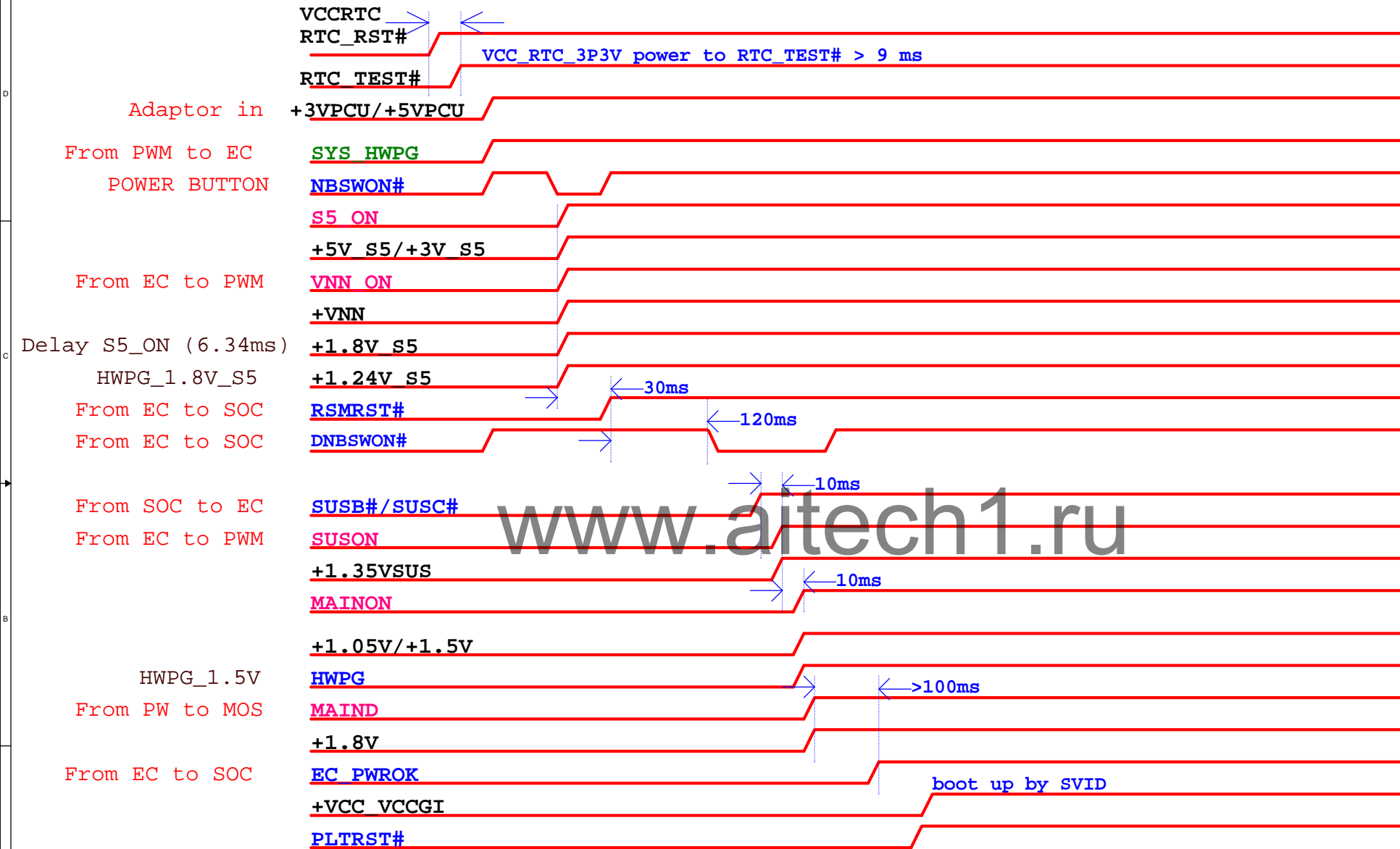


Quanta Computer Inc.

PROJECT : ZHVA

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Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF